PCB Design Engineers Introduction to High Density Semiconductor Package Technologies

2D, 2.5D and 3D System-in-Packaging and Ultra High-Density Hybrid Bond Interconnect

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Advanced 2D, 2.5D and 3D Packaging Technologies

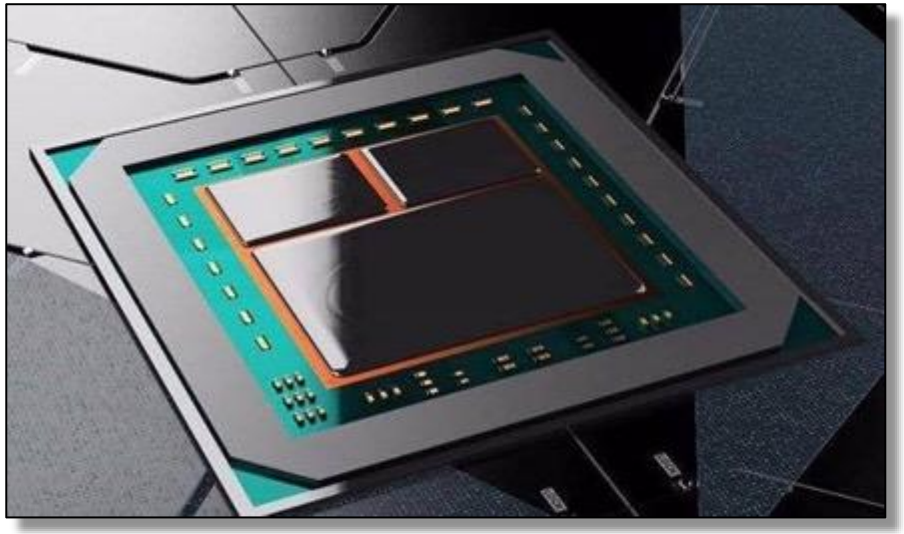


Image source: 3D In Cities

- 2D BGA Package Technology
- Implementing 2.5D for High-Density BGA Applications
- 3D and Hybrid Bond Interconnect Technologies

2D Microelectronics History

2D microelectronic technology has been used for decades to achieve package miniaturization goals using uncased die elements and 'hybrid' wire-bond assembly process methods.

- The 'hybrid microcircuit' is a miniaturized electronic circuit constructed of individual devices: semiconductor die elements, transistors, diodes and passive components, that are bonded to a metalized ceramic or silicon based substrate.

Die elements were traditionally terminated to the substrate using gold or aluminum wire-bond assembly processing.

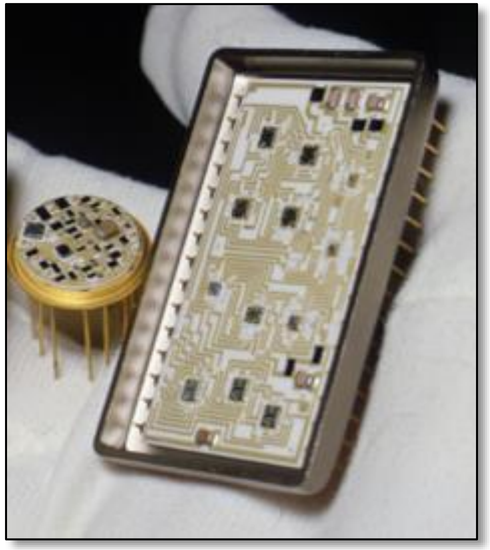


Image source: DHD Multimedia

Base Platform Materials for Traditional 2D Hybrid Microcircuit Technology

Image source: Teledyne Labtech

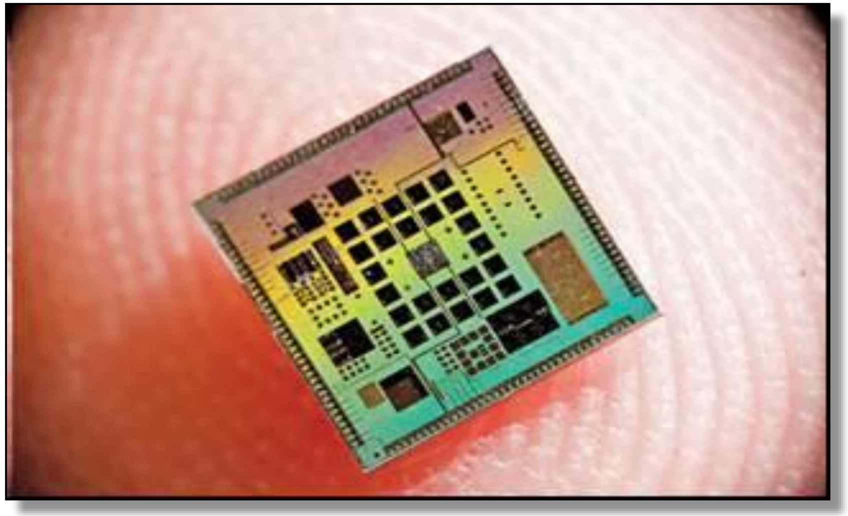
- ***Silicon***, generally furnished in a thin wafer (round) format that is passivated and metalized to provide the circuit pattern for component interconnect.
- ***Ceramic*** based dielectric panels are fabricated using low-temperature co-fired ceramic (LTCC) or high-temperature co-fired ceramic (HTCC) material.

Silicon Based 2D Microcircuit SiP

- 2D silicon-based microcircuits may include multiple bare die elements as well as a variety of miniature passive component functions.

Passive and active die elements may be formed or placed onto the interconnect substrate while in the wafer or panel format.

Die elements may be mounted in the face-up orientation for wire-bond interconnect or face-down (flip-chip) to accommodate reflow solder processing.



Source: Imperial College, London

Organic (FR-4) Based 2D Package Assembly

Other process variations have naturally evolved employing lower cost laminate base material and fabrication technologies.

- Clustering and interconnecting two or more associated heterogeneous or homogenous semiconductor die within the confines of a single BGA package outline enables closer coupling and the potential for maximizing electrical performance.

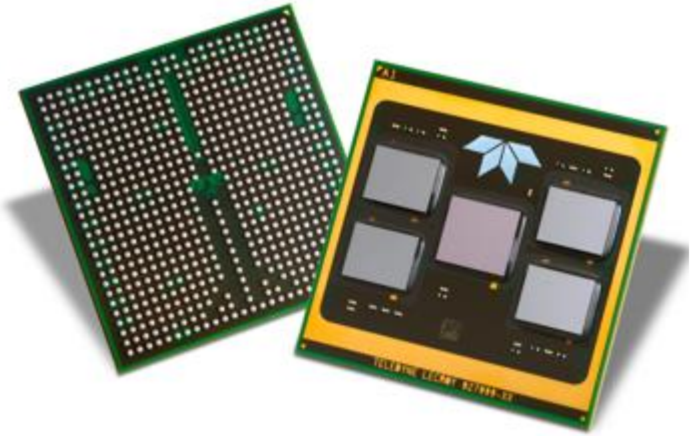


Image source: Teradyne

2D System-in-Package Advantage

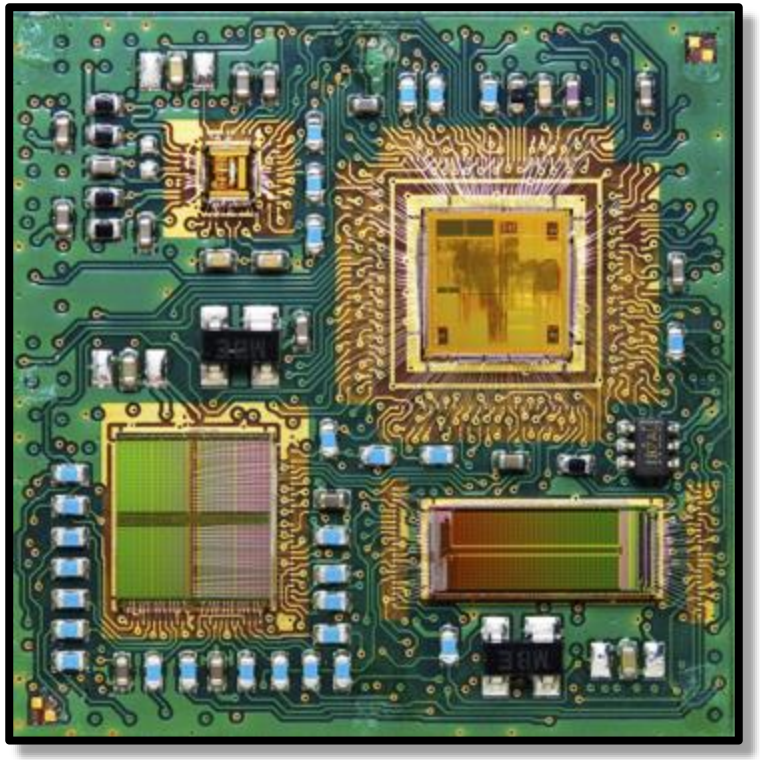


Image source: autodesk

A ‘system in package’, or SiP, is a way of bundling multiple ICs inside a single package outline.

This is in contrast to a ‘system on chip’, or SoC, where the functions on those chips are integrated onto the same die.

Key Benefit: The SiP provides quick development cycles, high levels of flexibility, and low development costs

System-on-Chip (SoC)

Apple's A17 Bionic has 16 billion transistors, the core circuitry elements that process and store data.

The semiconductor has a 16-core "neural engine," dedicated to speeding up artificial intelligence (AI) tasks.

It also has machine learning technology and includes photo recognition, focusing on faces in photos.

Image source: Apple

Comparing SoC to SiP Development Factors

SoC Approach: $1M – $1.5M per project

- Design Engineering: $500,000
- Frontend Process Engineering: $500,000
- Backend and Test Engineering: $350,000
- Projected Unit HVM Cost: $3.5
- Yield Loss in Early Stages: ~5%

SiP Approach: $500,000 - $800,000 per project

- Design Engineering: $200,000
- Packaging Engineering: $50,000
- Package Substrate Design: $150,000
- Test Engineering: $80,000
- Unit Cost Target: $3.5
- Yield Loss: ~2%

Data Source: Freescale

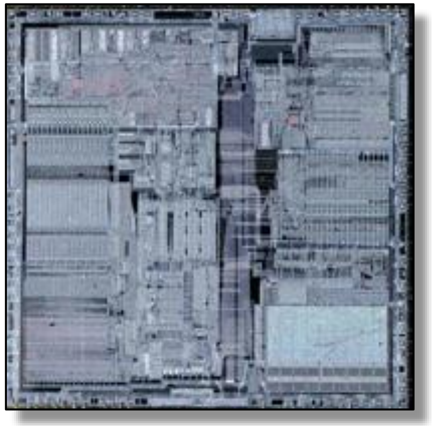


Image source: Octavo Systems

Issues impacting System-on-Chip Development

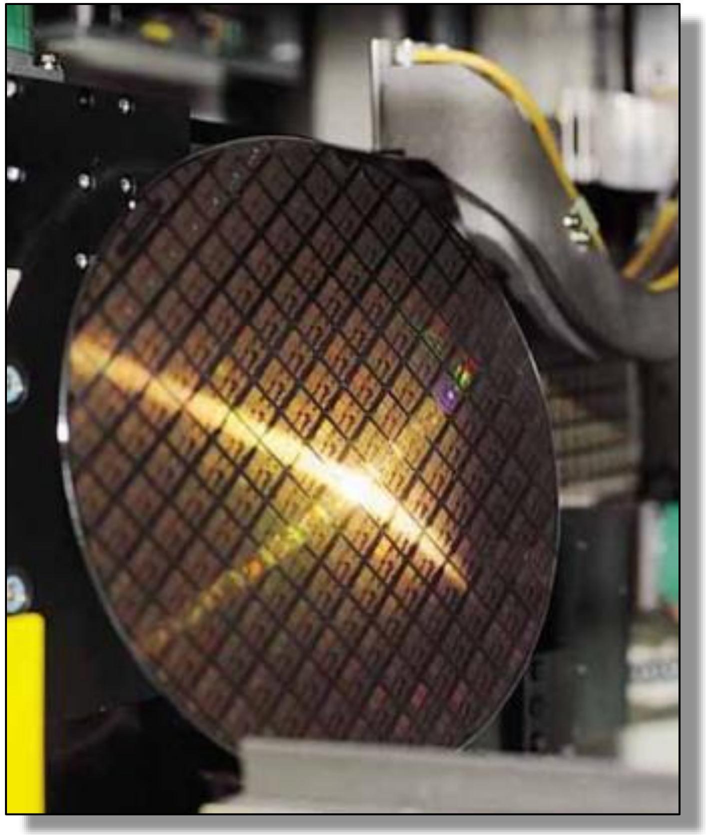


Image source:
Taiwan Semiconductor Manufacturing Co., Ltd

- The cost to remain on the leading edge has steadily increased with each generation of chips and the financial strain is being felt by both large merchant foundries and their fabless customers.
- To minimize development time and engineering cost, many merchant foundries have entered into joint ventures with their competitors in an effort to access existing IP, share research / design expenditures and minimize fab-maintenance expenses.

Current 2.5D System-in-Package Trends

A typical example of products currently in the market is Intel’s Xeon® 8180 2.5 GHz, Twenty-Eight Core Processor.

The company recently introduced their 12th Gen Intel Core i9-12900K, a 16 core desktop processor to support gamers and professional creators.

A number of semiconductor company’s position is that the 2.5D architecture represents a viable approach to both high I/O single-die, multiple-die and chiplet package applications.

So What is a 2.5D Semiconductor Package?

The 2.5D approach in packaging technology represents a significant advancement in semiconductor packaging, bridging the gap between traditional 2D and more advanced 3D methods.

Unlike 2D packaging, which generally demonstrates limitations in density and connectivity, the 2.5D method employs an innovative design strategy that incorporates an interposer separately from the active components.

The interposer allows for a more efficient chip connectivity!

Serving as a medium that facilitates more direct communication between multiple semiconductors placed on a single substrate, minimizing power consumption and significantly enhancing performance.

System Level Integration

Developing a multifunction semiconductor (SoC) for a specific product application requires a significant investment in both engineering and financial resources---

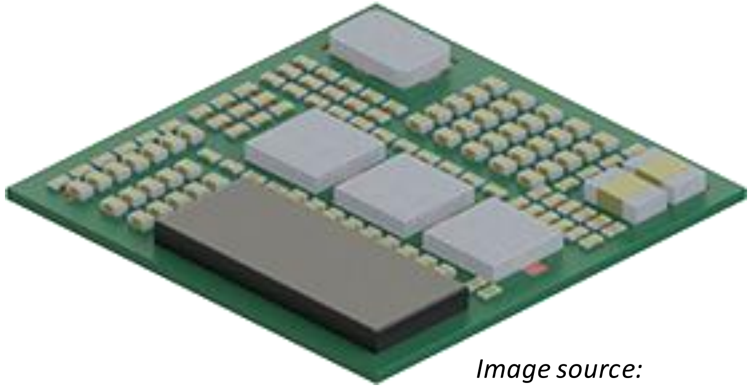
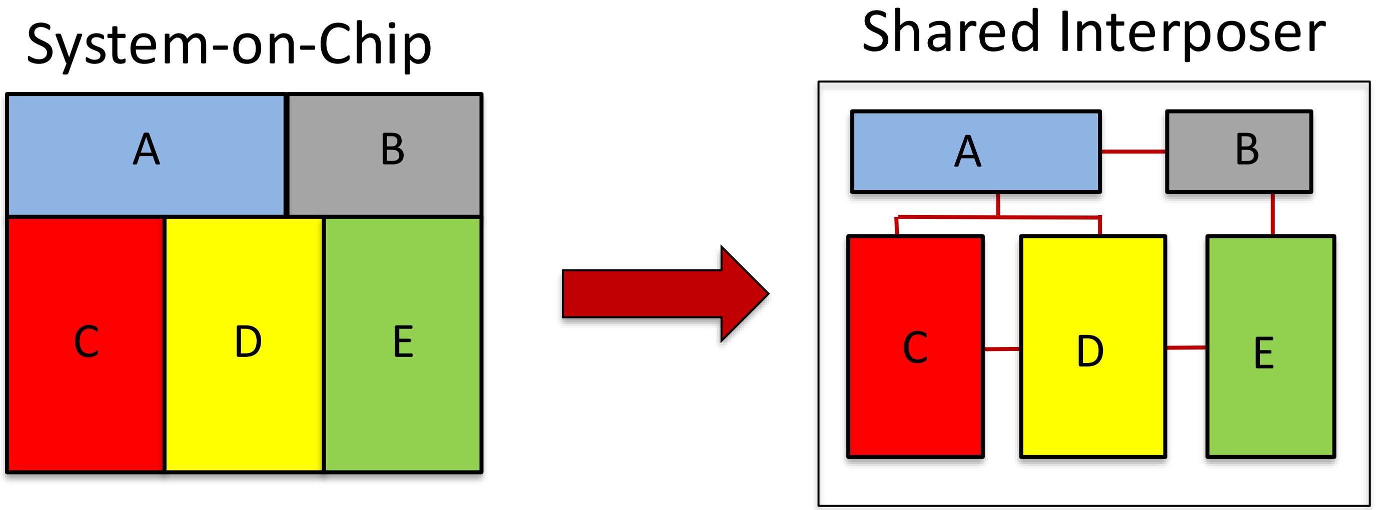


Image source: Amkor Technologies

A key goal is to control costs and develop packaging techniques that are not disruptive and ideally, utilize the existing manufacturing infrastructure.

To address these challenges, a number of alternative 2.5D and 3D semiconductor packaging solutions have evolved to enable faster transitioning from concept to volume manufacturing.

Drivers for Chiplet Integration

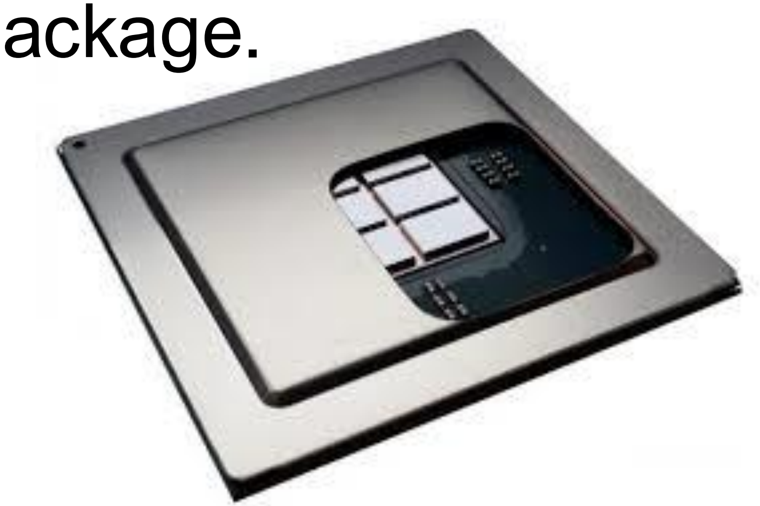


- Complex Integration
- Time Consuming
- Very Costly
- Low Initial Yield

- Die Source Flexibility
- Optimized Performance
- Reduced Time to Market
- Lower Development Cost

So What is a Chiplet?

- A chiplet is an integrated circuit ‘block’ that has been specifically designed to work with other similar chiplets' to form larger a more complex system level package.



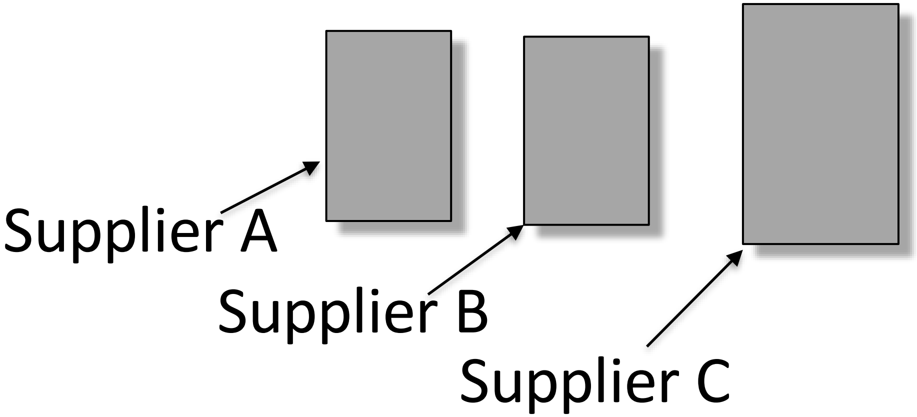
- Chiplets' allow manufacturers to increase yields of several smaller less complex functional chips over conventional monolithic CPU designs (where all functions are built onto a single piece of silicon for more direct interconnect).

LETI 96 –Core Chiplet Computer

Chiplet Based System-in-Packaging

- Mounting one or more uncased die elements to a high-density interposer enables much shorter interconnect for critical signal paths.
- With a majority of the interconnect accomplished on the interposers surface, the interface between the component(s) and package substrate is significantly less complex.
- This in turn allows the terminal pitch on the package substrate to increase and to simplify the design of the host PCB;
  - More efficient circuit routing
  - Reduced circuit layers
  - Improved power and ground distribution

2.5 D Heterogeneous 'Chiplet' Package Benefits



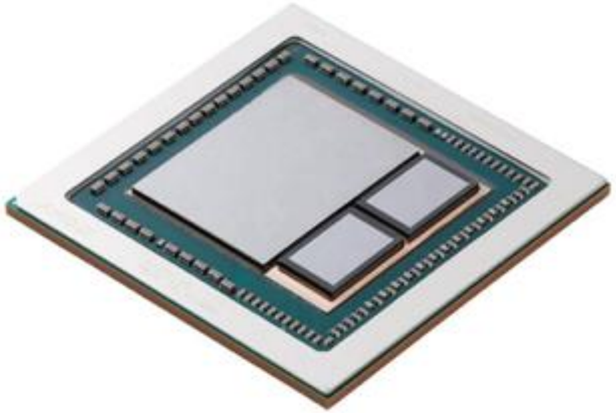


Image source: ASE Group

Logistics-

- Die sourcing flexibility
- Pre-tested die elements (KGD)
- Unlimited functional configuration
- Very fast development time

Performance-

- Shorter interconnect path
- Reduced power, inductance
- Increased speed
- Functionally in-socket testable

Status of Standards for Chiplet Semiconductor Packaging

JEDEC Announced the New Release of JEP30 Part Model Guidelines for Empowering Chiplet Integration

JEDEC guidelines show a standardized format compatible across various CAD tools to enable efficient communication and utilization of part models.

- Package Outline- The physical outlines of Chiplet packages are dynamic since they will depend on actual die size.
- Terminal Variations- Chiplet terminals may be furnished as flat lands, spheres, bumps or other protruding forms constructed from a variety of alloy and/or polymer materials.
- Terminal Layout- Chiplet package is defined by the matrix pitch and the offset of the central row(s) or column(s).

For more information, visit https://www.jedec.org.

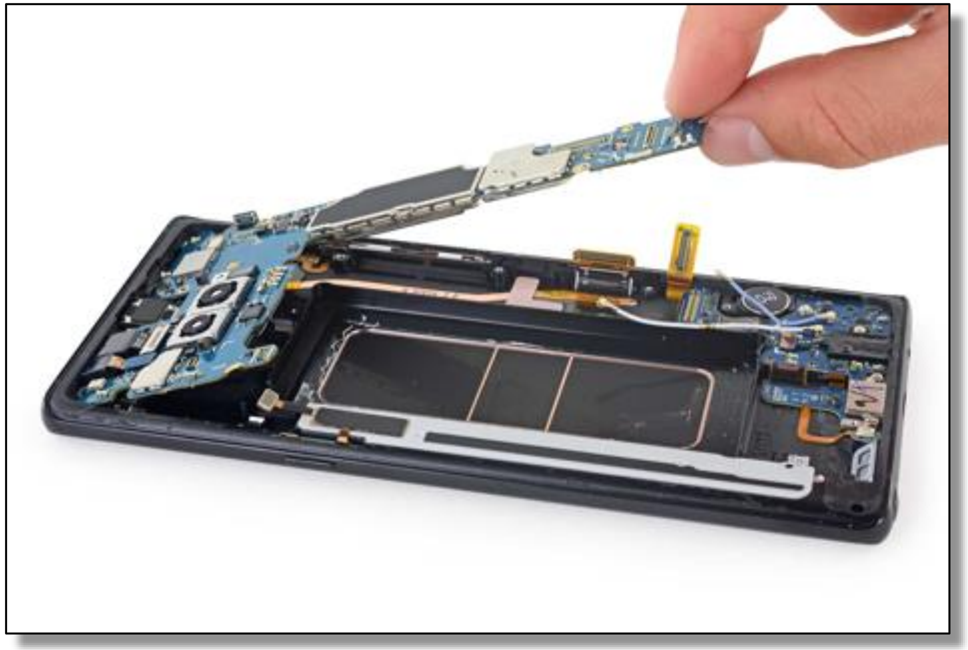
Implementing System Level Packaging

- A number of semiconductor assembly and test services (SATS) offer their customers assistance in developing a suitable package solution for diverse and very often complex applications.

Example source: STATSChipPac

Adapting proven semiconductor 'chiplet' die to meet the system level criteria can be economical and save development time but these products will frequently require sourcing these heterogeneous die elements from multiple sources.

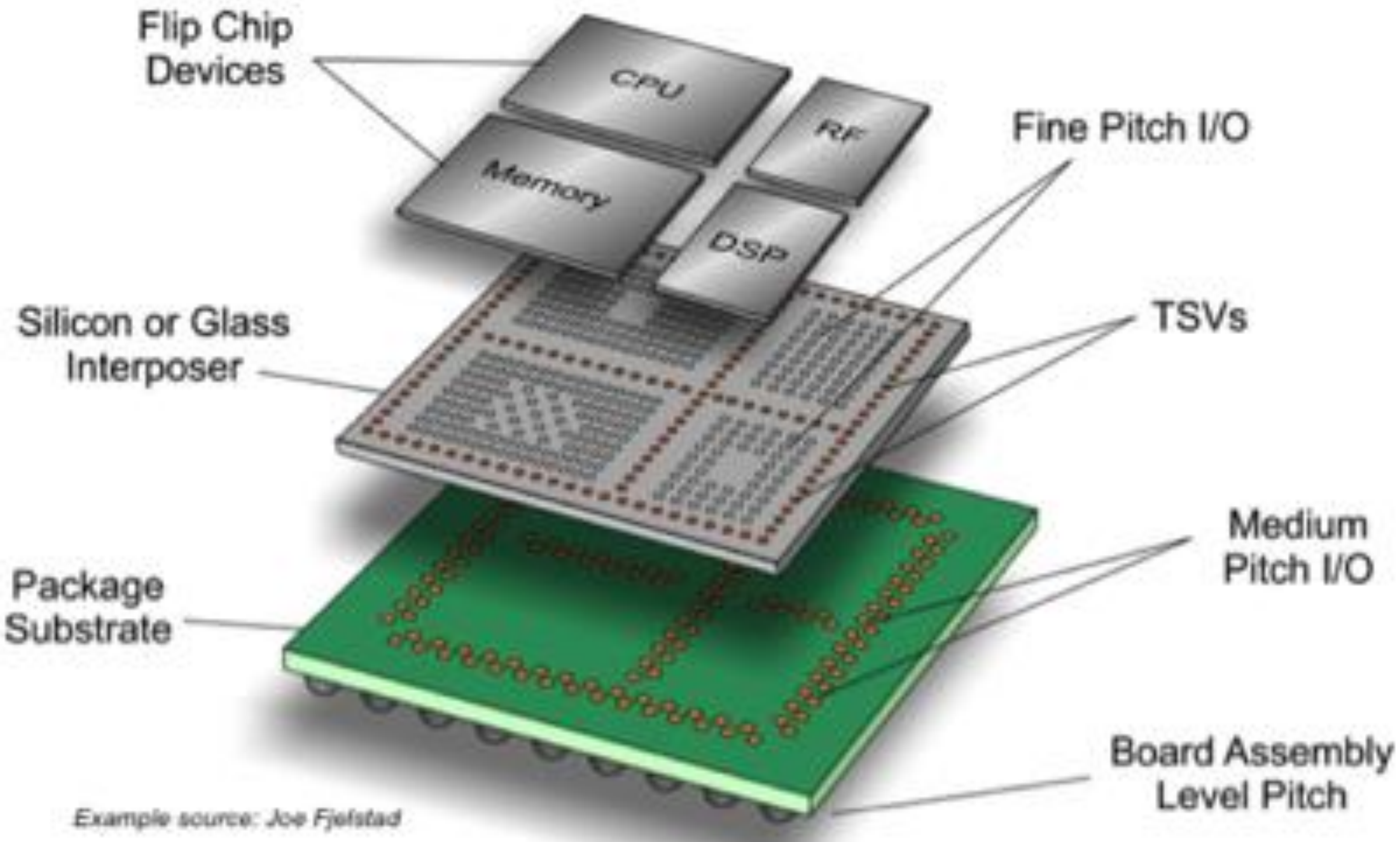
2.5D Interposer Design



Samsung Galaxy Note8 'Teardown'

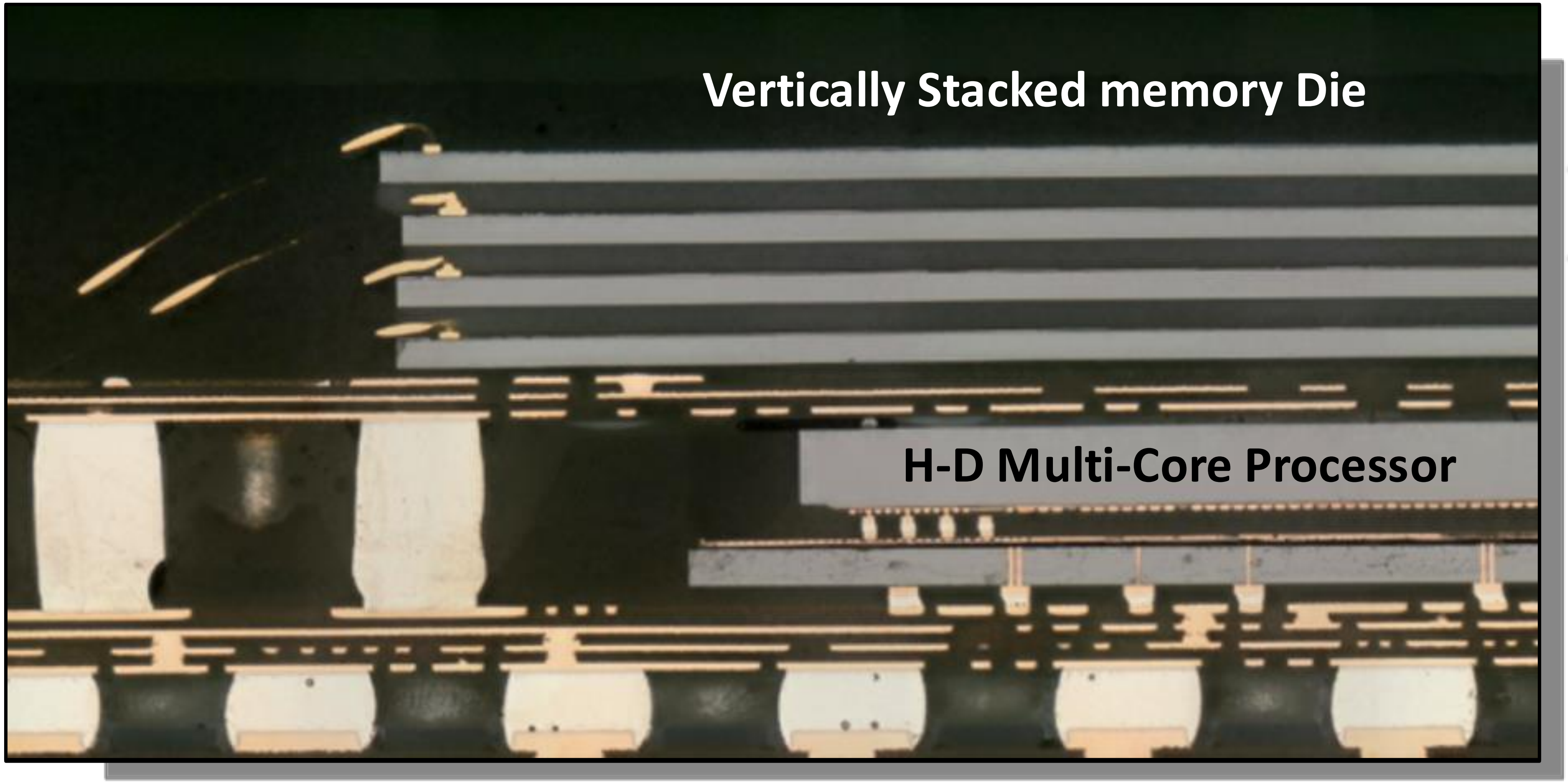
- The utilization of 3D packaging in high-function mobile/personal/consumer electronics enables the designer to develop a smaller PCB footprint and provide more space for all the other elements in the product that do not shrink very well (especially the battery).
- To address this movement, an increasing number of semiconductor die developed for advanced applications now require higher I/O with contact pitch variations that are significantly smaller than the mainstream semiconductor products previously in the market.

2.5D Silicon Based Interposer for High Density BGA Packaging



Example source: Joe Fjelstad

2.5D/3D System-in-Package Cross-Section



Memory die

Spacer

Level two substrate

H-D Logic die

Silicon interposer

Level one substrate

Intel Foveros 3D Packaging Technology

Interposer Panel Size Standards for System Level Integration

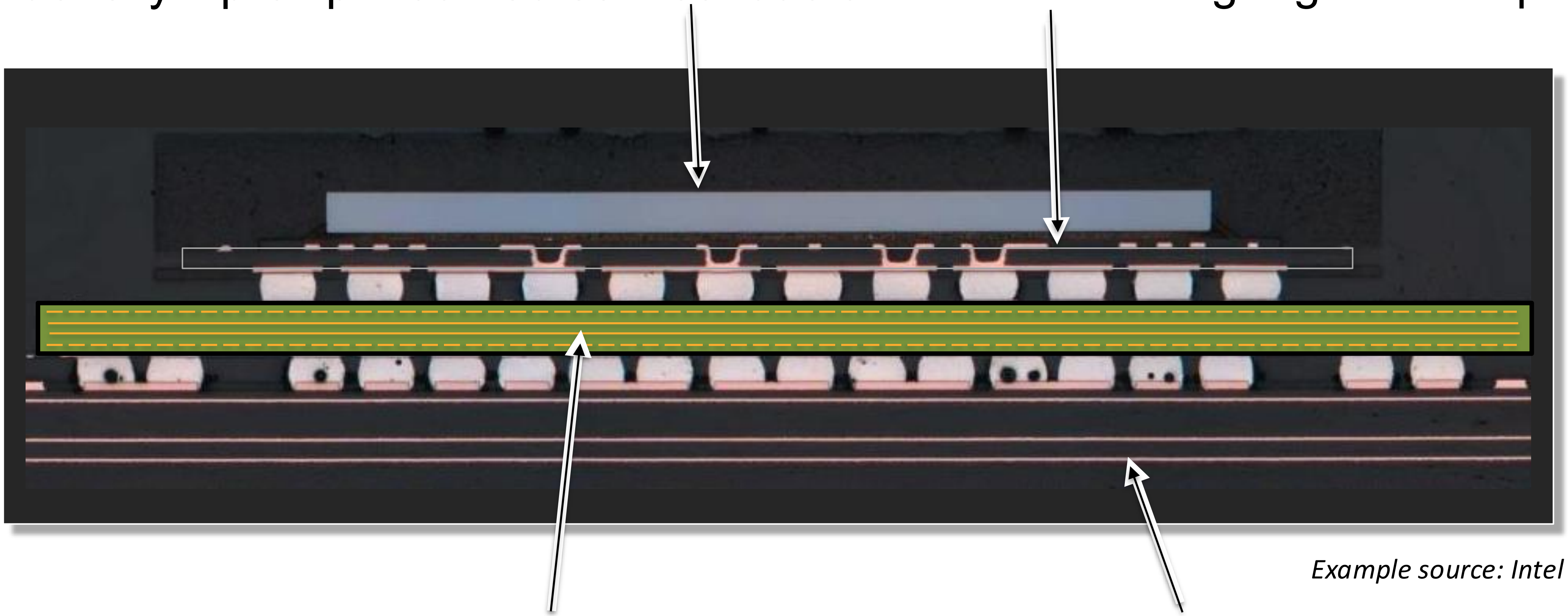
Semiconductor Equipment Manufacturing Industries (SEMI) Standards

SEMI Standards are developed by member companies with the goal of reducing manufacturing complexity and enable cost reduction, improve supplier quality, and reduce time-to-market.

- Epoxy-Based Material: 310 mm x 310 mm panel size
- Polymer-Glass Material: 310 mm x 310 mm panel size
- Silicon-Based Material: 300 mm diameter wafer size (traditional)

The 310 mm x 310 mm panel size is currently preferred by member companies- it can be processed with the existing wafer handling systems and maximizes unit population.

CTE Matching Organic Interposer Application



High density flip-chip mounted semiconductor

CTE matching organic interposer

Example source: Intel

B-T Epoxy package substrate

Host printed circuit board

Glass Reinforced Epoxy Interposers

- The core dielectrics can be furnished with a wide thickness range and copper foil variations.
- Via holes as small as 50-microns are typically formed using laser ablation technology and filled with copper prior to circuit imaging and chemical etching processes.
- Traditional chemically etched copper circuit fabrication technology currently enables conductor lines and spaces as narrow as 100-microns,
- For very fine line applications tha fabricator will employ semi-additive or fully additive copper plating processes similar to that used for silicon wafer RDL.

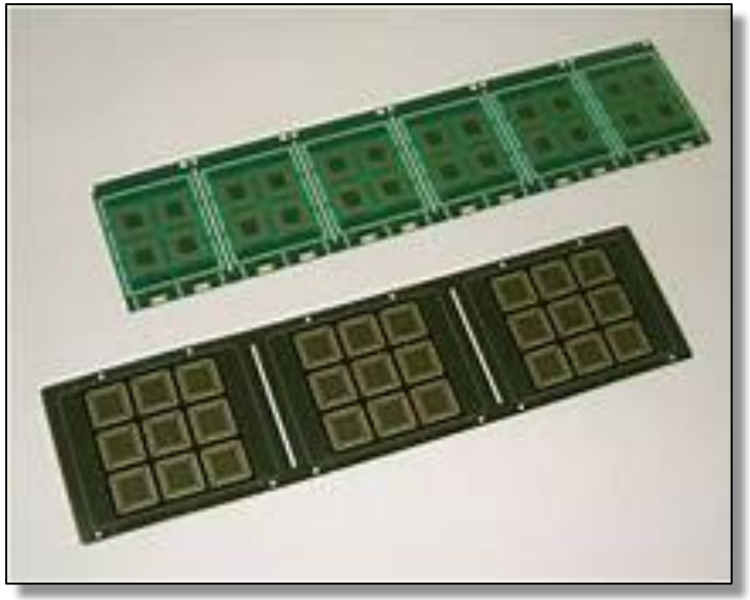
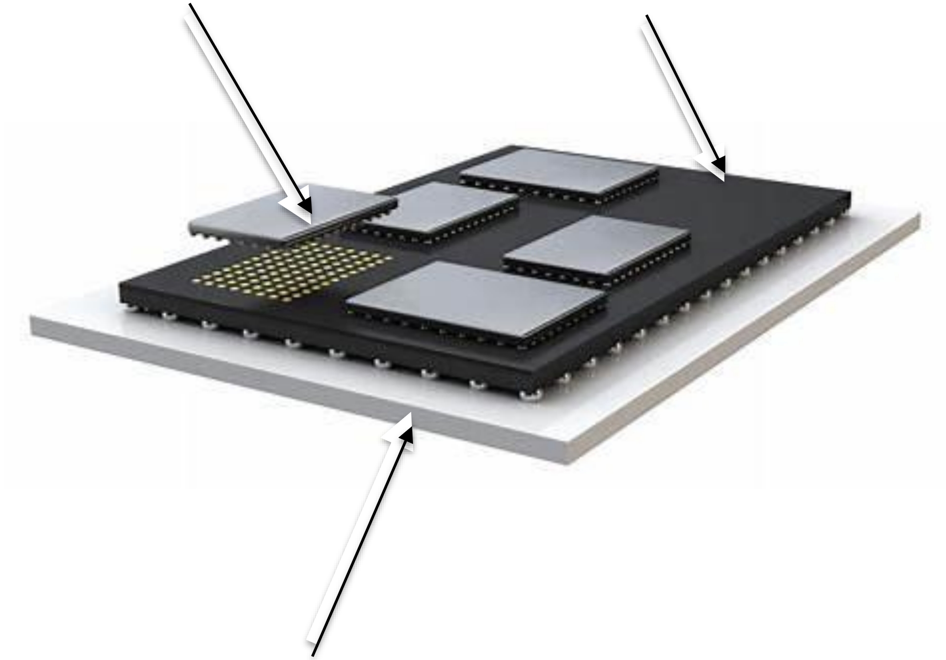


Image sources: Hwakwang, Korea and Hausermann Circuits, Austria

Polymer-Glass Core Interposers



High density flip-chip semiconductor set

Glass based interposer

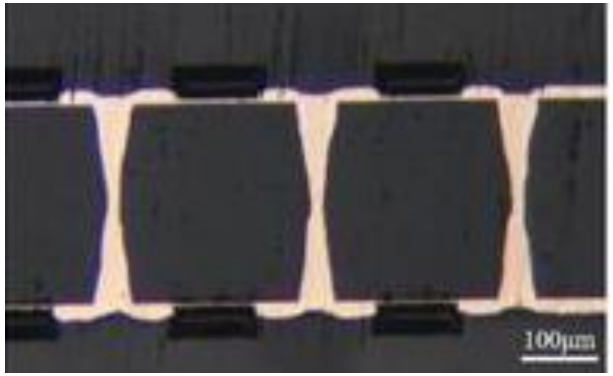
B-T Epoxy package substrate

Image source: Samtec Microelectronics

- Glass has gained momentum for interposer applications because it has a lower dielectric loss than silicon and its cost is significantly less than silicon.
- Regarding panel shape, panels are furnished at 310mm x 310mm to enable the use of existing die attach systems or board level SMT assembly systems.

Polymer-Glass Interposer Structures

Glass materials developed specifically for interposer applications are furnished in a thin round, square or rectangular format.



Electroless Cu filled TGVs

Image source: Vajra micro

- Via hole features on the die-attach side of the glass interposer may have a pitch in the range of 50 to 100-microns, while the terminal contact features on the bottom surface are commonly ‘fanned-out’ to a wider 200 to 300-micron pitch.

Via Forming Process for Polymer-Glass Interposers

The formation of through hole vias employ a combined laser and plasma etching technology.

- The laser introduces a modification in glass, weakening the glass structure in predefined areas, enabling increased etching rates in these modified areas.

This process is called laser induced deep etching.

The process does not create any cracks in the glass and allows the precise forming of both blind and through vias in glass, furnishing very high aspect ratios.

Typical via diameters are 20 - 100 microns and aspect rations are in the range of 1:4 to 1:10.

Through Glass Via (TGV) Fabrication Design Rules

TGV Design Rules		
Glass Panel	Thickness Range	200µm (.008”)
Through Glass Via Dia.	Min. Range	20 - 30µm (.001- .0014”)
Through Glass Via Dia.	Preferred	50µm (.002”)
Via Hole	C-C spacing	600µm (.024”)
Conductor	Lines and Spaces	2µm to 5µm
Layer Count	Top Surface	1 to 3
Layer Count	Bottom Surface	1

Data source: Asahi Glass

3D Die-to-Die, Die-to-Wafer, Wafer-to-Wafer Joining Process Variations

- Two primary joining methodologies currently being used for silicon-to-silicon interconnects are:
    1) Reflow solder
    2) Hybrid bonding

Hybrid memory cube:
Micron Technology

Joining Vertically Stacked, TSV Configured Memory Die

- A relatively high temperature Tin alloy based solder composition is plated or deposited onto the copper terminal surfaces.
- Flux is applied to opposing surfaces and die elements aligned and sequentially stacked onto each other.
- Reflow solder processing completes the joining process followed by flux residue removal and polymer underfill.

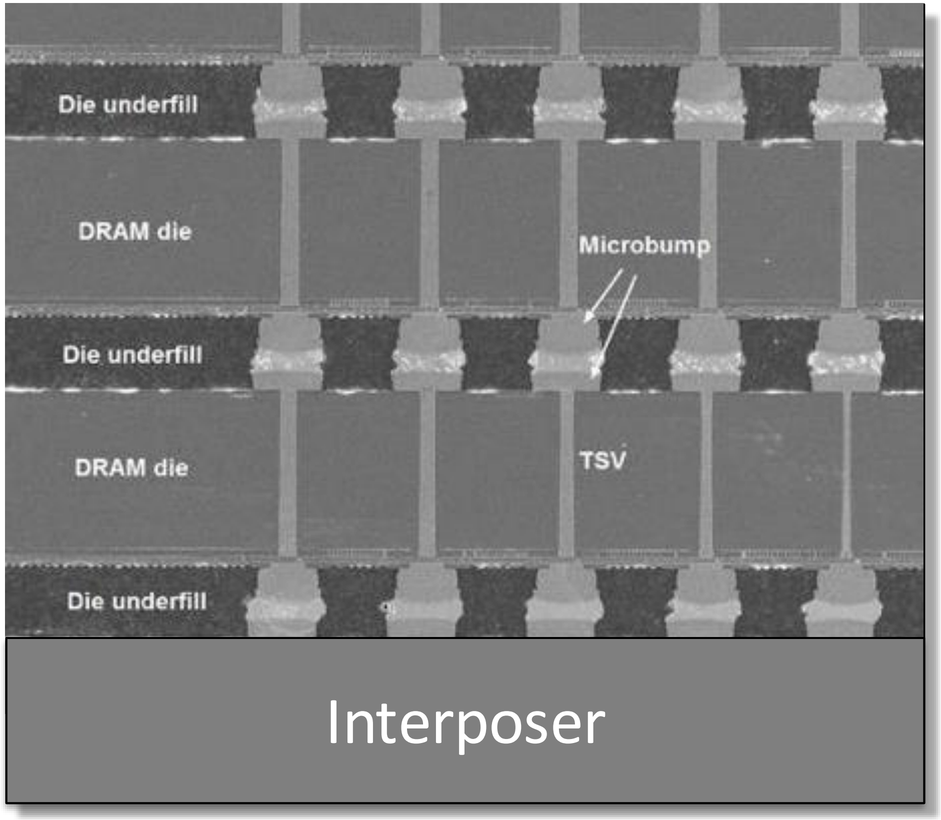
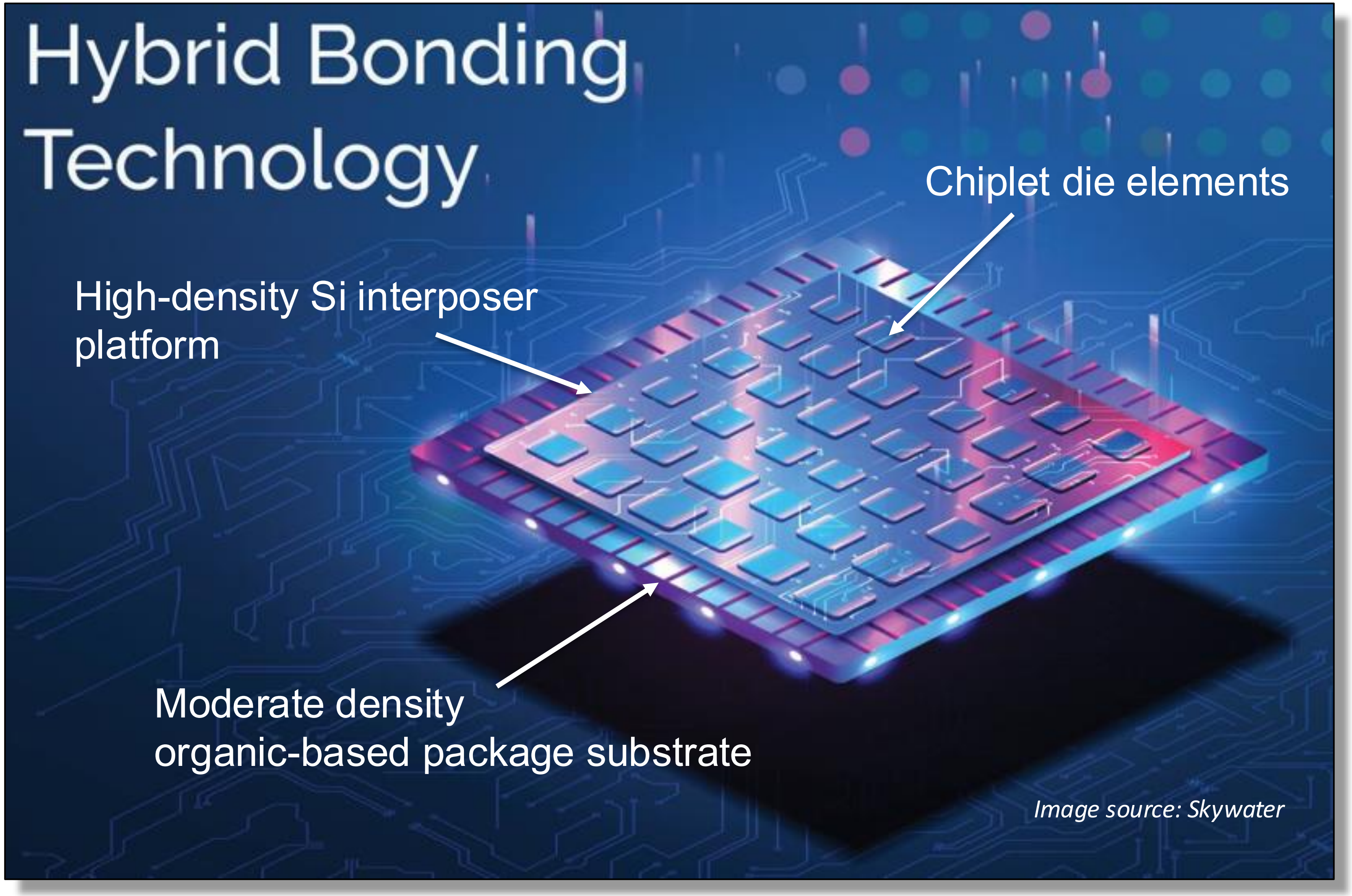


Image source: SK Hynix



Hybrid Bonding Technology

Chiplet die elements

High-density Si interposer platform

Moderate density organic-based package substrate

Image source: Skywater

Hybrid Bonding

Hybrid bonding is a heterogeneous integration platform technology that enables vertical joining of semiconductor die-on-wafer, die-on-die and even wafer-on-wafer without solder or other additive conductive materials.

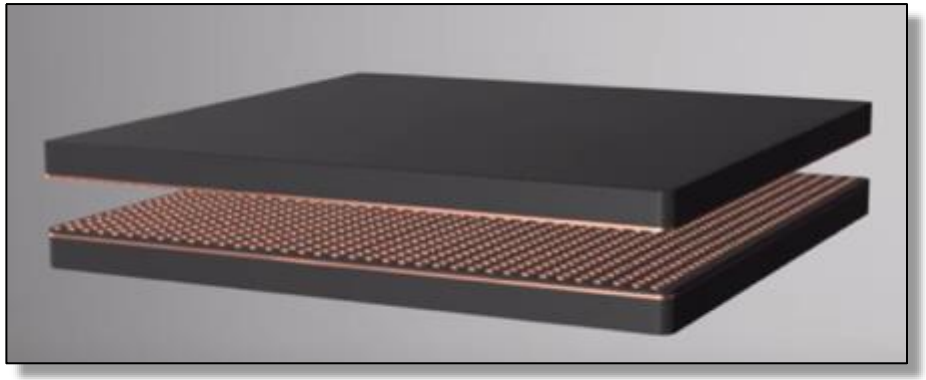


Image source: Adeia

The technology is increasingly being utilized for joining various semiconductor devices such as sensors, memory, and logic devices, enabling enhanced performance and increased functionality while reducing overall package size and manufacturing cost.

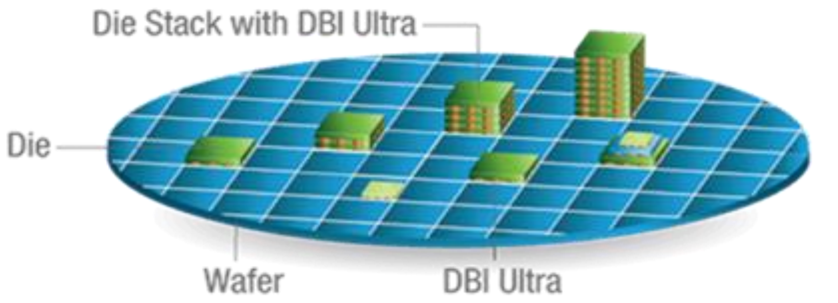
Hybrid bonding is now recognized industry-wide as direct bond interconnect (DBI).

The DBI process promotes bonding between apposing copper terminals to enable the face-to-face connection for:

- Wafer-to-wafer joining (W2W)
- Joining die elements onto wafers (D2W)
- Joining die onto die (D2D)

Note: The DBI process does not require solder and flux to promote joining, eliminating the need for post process cleaning and underfill application.

Direct Bond Interconnect (DBI ®) Technology



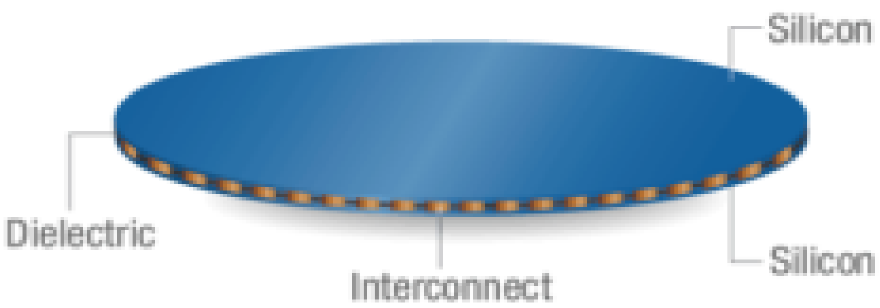


Image source: Adeia

Die-on-Die DBI Joining- Ideal for vertically stacking multiple memory die.

Die-on-Wafer DBI Joining- Efficient integration solution for multiple die SiP applications.

Wafer-to-Wafer DBI Joining- Applications include BSI Image Sensor, DRAM, MEMS, RF, and a multitude of consumer electronics

Note: Adeia, a technology development and licensing company in Santa Clara, California, has contributed in the development, adoption and implementation of the hybrid bonding process, licensing their DBI technology to major foundries and IDMs.

DBI ® Wafer-to-Wafer Hybrid Bonding

DBI® is an enabling low-temperature, low profile die-to-wafer and die-to-die hybrid bonding technology platform.

- By eliminating the need for copper pillars and underfill, DBI enables a dramatically thinner stack as compared to conventional approaches.
- DBI also allows the stacking of die that are the same or different sizes, processed on fine or coarse wafer process technology nodes.
- They may be manufactured on the same or different wafer sizes while readily scaling down to 1 µm interconnect pitch, providing the ultimate 2.5D and 3D integration flexibility.

DBI ® Wafer-to-Wafer Bonding Process

During processing, the embedded metal bond pads (typically copper or nickel), are polished to form a slightly dished surface with minimal roughness.

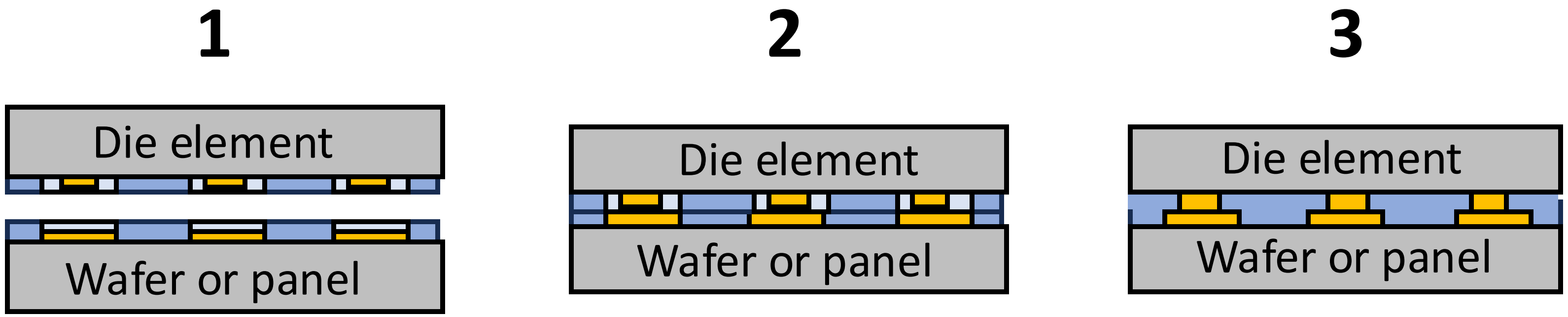
The prepared wafers are then aligned and placed together, resulting in the spontaneous formation of strong chemical bond between the prepared surfaces.

After a moderate batch anneal, the DBI bond pads expand together to form a homogeneous metallic interconnect with grain growth across the bond interface.

The chemical bond between oxides is significantly strengthened, ensuring high reliability without requiring underfill.

Note: Polishing and dishing are achieved using standard chemical mechanical polishing (CMP) tools and nitrogen-based chemistries are applied through conventional plasma etch methods.

DBI Cu-Cu Oxide bond joining Process Sequence



1. Align and place die onto Si or glass based interposer surface
2. After die placement, there is a spontaneous bond between oxide layers
3. Cu-Cu interconnect forms at elevated temperature (without external pressure)

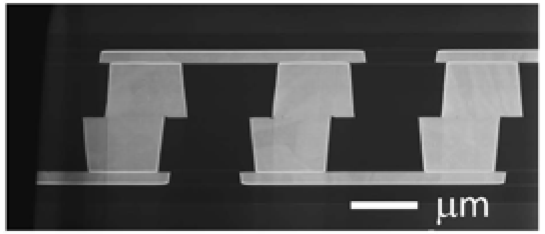
Interdiffusion of the Cu pads requires time at temperature to complete the metallurgical bond. Since the initial oxide bonding also takes place at room temperature, Cu oxidation during bonding is minimized.

Direct Bond Interconnect (DBI)

DBI® is a low temperature hybrid direct bonding technology that allows wafers to be bonded with exceptionally fine-pitch electrical interconnect.

- The DBI alignment and bonding process is performed at room temperature.

Cross Section

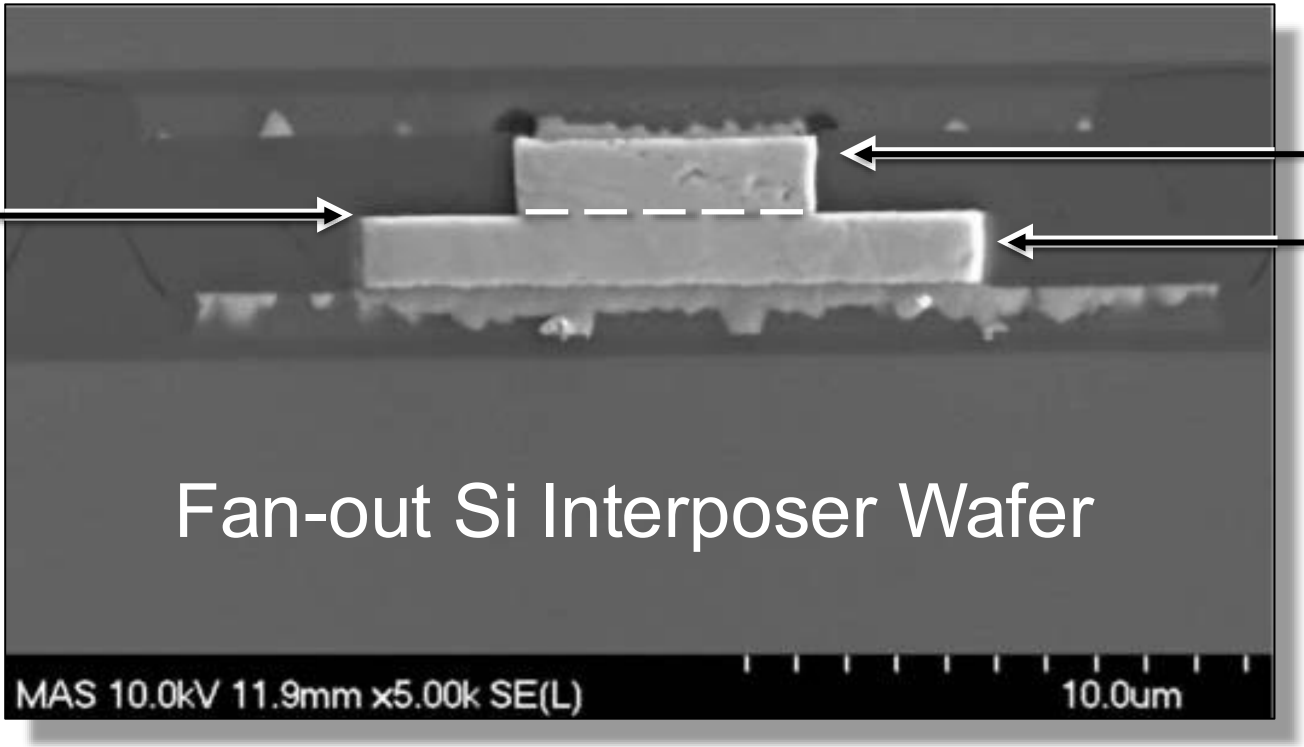


Features

Bond Metal	Cu, Ni
Bond Pad Size	<1um to 20um
Low Temperature	~150 c
Compatible Dielectrics	Si_xO_y, $Si_xO_yN_z$, $Si_xC_yN_z$

The process leverages industry-standard wafer bonding equipment, enabling the high-throughput, low cost-of-ownership fabrication process required for high volume market applications.

Post DBI® Oxide Process View



Die element

Oxide Bond interface

Copper land on die element

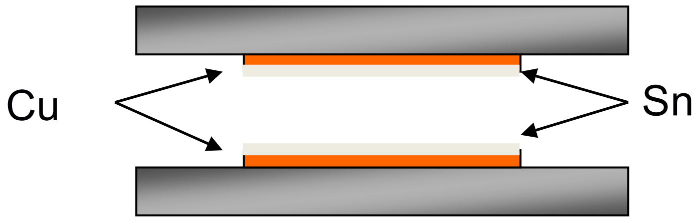
Copper land on wafer surface

Image source: Ziptronix

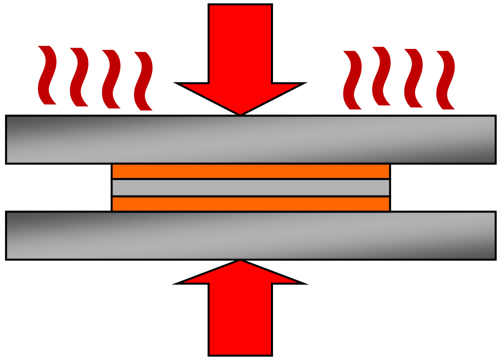
Note: In 2015, Tessera Technologies, an Adeia member company in Santa Clara California, acquired Ziptronix and added the z-bond process to their DBI IP portfolio.

Alternative Hybrid (Fusion) Bond Sequence

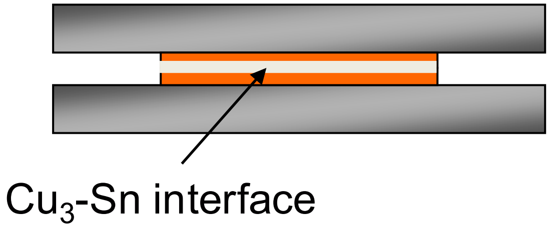
- A thin layer of tin (Sn) is first applied onto the exposed copper terminal features.
- The joining process is a two-stage procedure that begins with precise alignment and pre-bonding of the die elements at room temperature .
- Following pre-bond, the stacked die elements or wafers are exposed to an annealing process that includes both high temperature and high pressure.



Align Die



Apply heat and pressure



Bonding complete

Post Fusion Bond View

- When the stacked die or wafers are heated to approximately 400ºC, the tin alloy will completely diffuse into apposing copper land features to form a stable Cu-Sn-Cu (Cu_3Sn) intermetallic at the land-to-land interface.

Image of the bond between wafer pairs

Image source: Qimonda

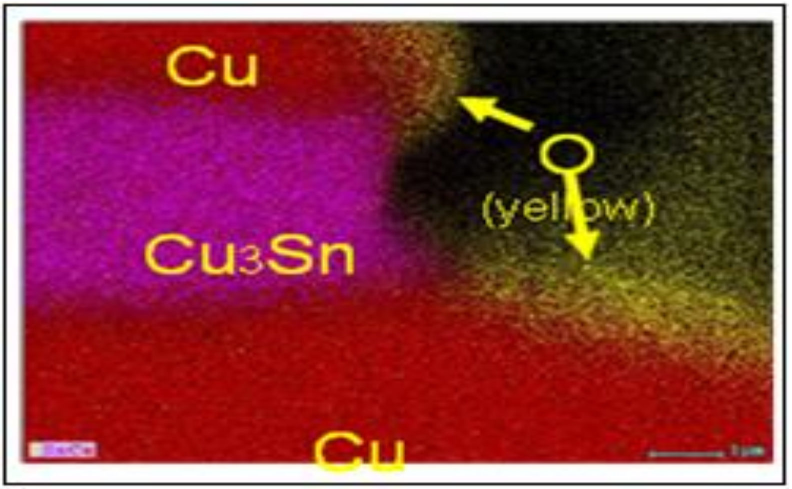


Image source: Invensas

Key Advantages and Benefits of DBI

- Significant benefits in product performance
- Greater interconnect density, and bandwidth
- Energy efficient and enhanced thermal performance
- Improved signal integrity, and interconnect reliability
- Hybrid bonding is a low-temperature joining technology

The maturity of the process technology has lead to higher process yields enabled by a robust manufacturing infrastructure.

DBI Process Challenges

Manufacturing process related challenges-

- Aligning small diameter copper terminal columns
- Electrochemical deposition (ECD) plating complexity
- Controlling terminal co-planarity.
- Surface roughness and hardness
- Temperature, time and pressure control

The risk of intermetallic compound formation that may compromise conductivity and mechanical joining properties.

Terminal to DBI Land Diameter Consideration

Terminal Pitch (e)		10.0 µm	8 .0 µm	6 .0 µm	4 .0 µm	2.0 µm	1.5 µm	1.0 µm	< 1.0 µm
Terminal Diameter		5.0 µm	4.0 µm	3.0 µm	2.0 µm	1.0 µm	0.75 µm	0.50 µm	TBD
Cu Land Diameter		5.0 µm	4.0 µm	3.0 µm	2.0 µm	1.0 µm	0.75 µm	0.50 µm	TBD
Cu Land + Tolerance		5.5 µm	4.5 µm	3.5 µm	2.5 µm	1.25 µm	1.0 µm	0.75 µm	TBD
Single Conductor		1.6 µm	1.3 µm	1.0 µm	0.6 µm	0.3 µm	0.25 µm	0.16 µm	TBD
Two Conductors		1.0 µm	0.80 µm	0.60 µm	0.40 µm	0.20 µm	0.15 µm	0.10 µm	TBD

Key Planning Issues for 2.5D and 3D Packaging

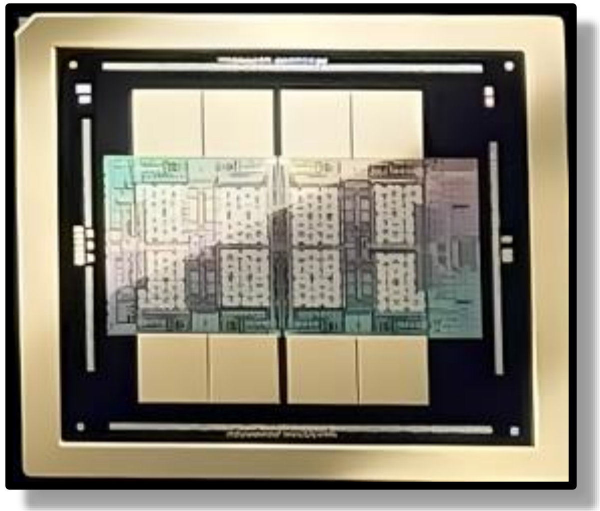
There continues to be great deal of progress in multiple die package process refinement and system development, however, methodologies will vary a great deal.

Some of the issues that will need to be resolved include;

- Selection of suitable semiconductors for multiple die packaging
- Establishing reliable sources for semiconductor elements
- Specifying physical and environmental operating conditions
- Defining package design constraints and process protocols
- Stipulating electrical test method and post assembly inspection criteria.

Challenging Days Ahead…

- While developers continue to explore alternative semiconductor package assembly methods, significant challenges remain for the PCB designer–
  - For example, new memory products have emerged with 30-micron terminal pitch features, some having up to two thousand I/O and processors have entered the market that have as many as *forty thousand* I/O.



NVIDIA's Rubin GPU

Final note…

High-density system level packaging is evolving-

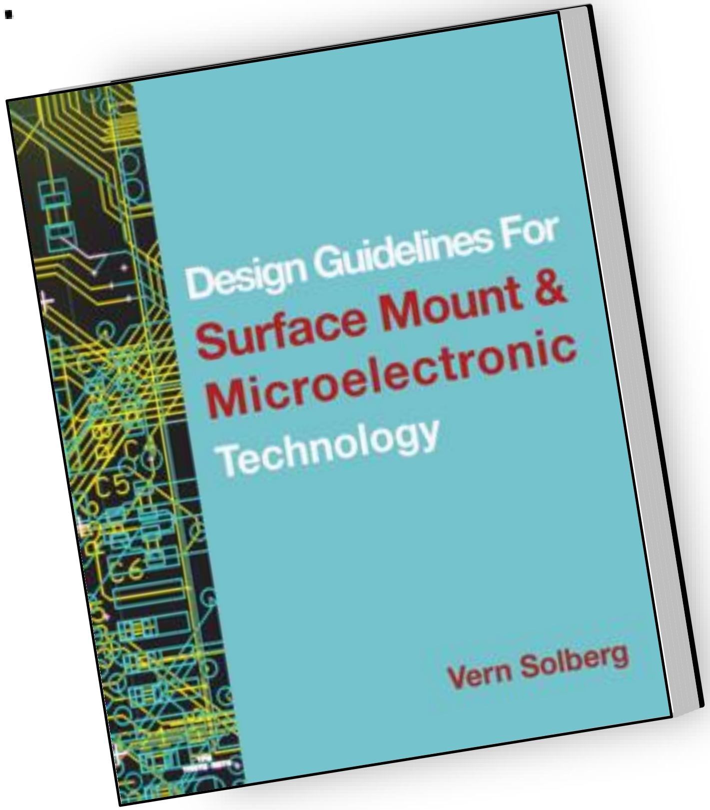
- Significant challenges remain for PCB design specialists when adopting the newer generations of very high-density and high I/O semiconductors.
- In order to meet the requirement for interconnecting these high terminal density die elements, analysts and industry roadmaps predict that many companies may migrate toward the silicon or glass based interposer technology.

On the other hand, the ultra-low CTE, organic-based interposer fabrication technology will be a strong alternative because it is significantly lower in cost than silicon or glass and the PCB fabrication infrastructure is already well established globally.

Publications Available for Design and Process Implementation

- **IPC-7095** describes the design and assembly criteria for implementing ball grid array (BGA and FBGA) technology
- **IPC-7094** defines the design and assembly challenges for implementing flip-chip and die size component technology.
- **IPC-7091** furnishes design and assembly process solutions for implementing a wide range of 3D component technologies.
- **Design Guidelines for Surface Mount and Microelectronics**

Design Guidelines for Surface Mount and Microelectronics



Each section of the book is written, illustrated and detailed to guide the user in the implementation of process-proven SMT and microelectronic packaging methods and techniques.

This book provides the reader with step-by-step procedures in developing the most cost-effective product possible.

Also defined are details related to device standards, alternative semiconductor packaging methods, and high-density circuit board fabrication options.

Available in hard cover and soft cover from
Amazon.com or **SOLBERG**TECH.com

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